



# **COMPUTER ORGANIZATION AND ARCHITECTURE**

**For  
COMPUTER SCIENCE**



# COMPUTER ORGANIZATION AND ARCHITECTURE

## SYLLABUS

Machine instructions and addressing modes, ALU and data-path, CPU control design, Memory interface, I/O interface (Interrupt and DMA mode), Instruction pipelining, Cache and main memory, Secondary storage.

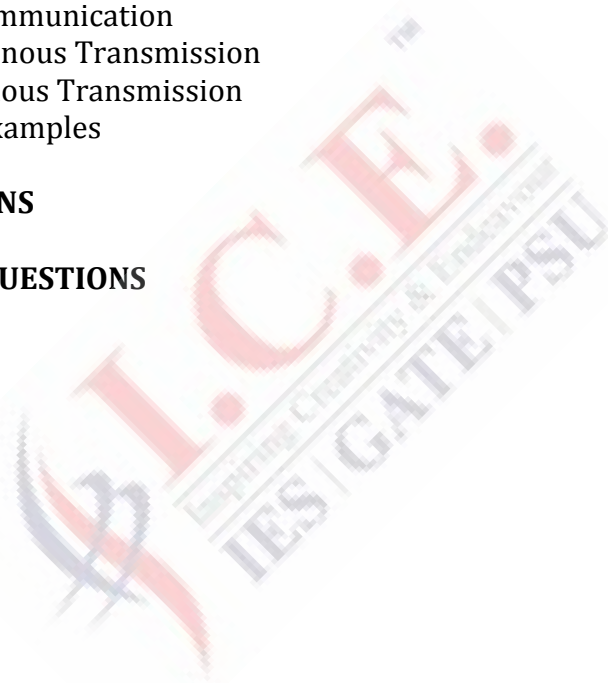
## ANALYSIS OF GATE PAPERS

Exam Year	1 Mark Ques.	2 Mark Ques.	Total
2003	2	3	8
2004	1	7	15
2005	4	8	20
2006	1	7	15
2007	2	6	14
2008	-	12	24
2009	2	4	10
2010	1	4	9
2011	1	4	9
2012	2	2	6
2013	1	4	9
2014 Set-1	1	3	7
2014 Set-2	1	3	7
2014 Set-3	1	2	5
2015 Set-1	1	1	3
2015 Set-2	1	2	5
2015 Set-3	1	2	5
2016 Set-1	1	2	5
2016 Set-2	1	5	11
2017 Set-1	4	5	14
2017 Set-2	4	3	10

# CONTENTS

Topics	Page No
<b>1. OVERVIEW OF COMPUTER SYSTEM</b>	
1.1 Introduction	01
1.2 Functional Units	01
1.3 Numbers and Arithmetic Operations	02
1.4 Decimal Fixed-Point Representation	04
1.5 Floating Point Representation	04
1.6 Signed-Operand Multiplication	05
1.7 Booth's Algorithm	05
1.8 Integer Division	06
1.9 Non-Restoring-division Algorithm	07
1.10 Flouting-Point Numbers and Operations	07
<b>2. INTRODUCTIONS</b>	
2.1 Introduction cycle	13
2.2 Addressing Modes	14
2.3 Instruction Formats	14
2.4 Instruction Interpretation	17
2.5 Microgram med Control	19
2.6 Wilkes Design	19
2.7 Horizontal and Vertical Microinstructions	20
<b>3. MEMORY ORGANIZATION</b>	
3.1 Introduction	22
3.2 Memory Hierarchy	22
3.3 Memory Characteristics	25
3.4 Semiconductor Ram Memories	26
3.5 Virtual Memory Technology	35
3.6 Advantages of using Virtual Memory	36
3.7 Paging, Segmentation and Paged Segments	37
3.8 Secondary Memory Technology	40
<b>4. INPUT AND OUTPUT UNIT</b>	
4.1 I/O Mapping / Addressing Methods	44
4.2 IOP (IO Processor)	45
4.3 Direct memory Access	46
4.4 Steps involved in the DMA operation	48
4.5 Interrupt-Initiated I/O	50
4.6 Data Transfer Techniques	50

4.7	Responsibilities of I/O Interface	52
4.8	IBM 370 I/O Channel	53
4.9	Polling	55
4.10	Independent Requesting	55
4.11	Local Communication	56
<b>5.</b>	<b>MULTIPLE PROCESSOR ORGANISATION</b>	
5.1	Flynn's Classification of Computer Organization	60
5.2	Multiprocessor	61
5.3	Parallel Processing Applications	61
5.4	Multiprocessor Architecture	62
5.5	Loosely Coupled Multiprocessor	62
5.6	Serial Communication	63
5.7	Asynchronous Transmission	63
5.8	Synchronous Transmission	64
5.9	Solved Examples	64
<b>6.</b>	<b>GATE QUESTIONS</b>	66
<b>7.</b>	<b>ASSIGNMENT QUESTIONS</b>	100

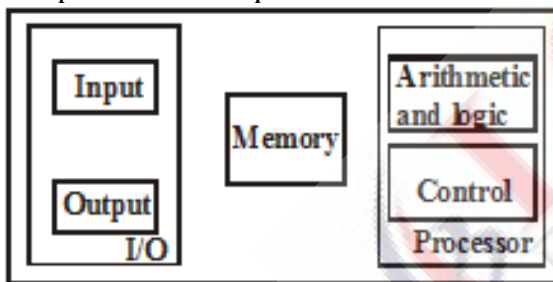


## 1.1 INTRODUCTION

**Digital computer or simply computer** is fast electronic calculating machine that accepts digitized input information processes it according to a list of internally stored instructions, and produces the resulting output information. The list instruction is called a computer program, and the internal storage is called computer memory. Many types of computers exist that differ in many factors like size, cost, computational power and intended use.

## 1.2 FUNCTIONAL UNITS

A computer consists of five functionally independent main parts:



Basic functional units of a computer

### 1.2.1 Input unit

- Accepts coded information from human operators, from electromechanical devices such as keyboards, or from other computers over digital communication lines.
- Many other kinds of input devices are available, including Joysticks, Trackballs, and mouses. These are often used as graphic input devices in conjunction with displays.

### 1.2.2 Memory Unit

- The function of the memory unit is to store

program and data. There are two classes of storage, called primary and secondary.

- Primary storage is a fast memory that operates at electronic speeds. Programs must be stored in the memory while they are being executed.
- The memory contains a large number of semiconductor storage cells, each capable of storing one bit of information.
- Programs must reside in the memory during execution. Instructions and data can be written into the memory or read out under the control of the processor.

Memory in which any location can be reached in a short and fixed amount of time after specifying its address is called random-access-memory (RAM).

- The time required to access one word is called the memory access time. This time is fixed, independent of the location of the word being accessed.
- The small, fast RAM units are called caches, they are tightly coupled with the processor and are often contained on the same integrated circuit to achieve high performance.
- The main memory is largest and slowest unit. Although primary storage is essential, it tends to be expensive. Thus, additional cheaper, secondary storage is used when large amounts of data any many programs which are infrequently used have to be stored.

### 1.2.3 Arithmetic and Logic Unit

- Most of the operations are executed in the arithmetic and logic unit (ALU) of the processor.

**For example:** for addition of two numbers, they are brought into the processor, and the actual addition is carried out of the ALU.

- Any other arithmetic or logic operation, like multiplication, division is initiated by bringing the required operands into the processor, where the operation is performed by the ALU.
- The control and the arithmetic and logic units are many times faster than the other devices connected to a computer system. This enables a single processor to control a number of external devices such as keyboards, displays, magnetic and optical disks.

### 1.2.4 Output Unit

The output unit is the counterpart of the input unit. Its function is to send processed results to the outside world. For example: printers.

### 1.2.5 Control Unit

- The memory, arithmetic and logic, and input and output units store and process information and perform input and output operations. The control unit is effectively the centre that sends control signals to other units and senses their states.

### The operation of a computer:

- The computer accepts information in the form of programs and data through an input unit and stores it in the memory.
- Information stored in the memory is fetched, under program control, into an arithmetic and logic unit, where it is processed.
- Processed information is output through a output unit and all activities inside the machine is directed by the control unit.

## 1.3 NUMBERS & ARITHMETIC OPERATIONS

Computers are built using logic circuits that operate on information represented by two values as 0 and 1 and we define the amount of information as a bit information.

### 1.3.1 Number Representation

Consider an n-bit vector

$$C = C_{n-1} \dots \dots \dots C_1 C_0$$

Where  $C_i = 0$  or  $1$  for  $0 \leq i \leq n-1$ . This vector can represent unsigned integer values  $V$  in the range  $0$  to  $2^n-1$ , where

$$V(C) = C_{n-1} \times 2^{n-1} + \dots + c_1 \times 2^1 + c_0 \times 2^0$$

Three systems are used for representing the positive and negative numbers:

#### 1. Sign and Magnitude

- The leftmost bit is 0 for positive numbers and 1 for negative numbers.
- In this, negative values are represented by changing the most significant bit from 0 to 1 in the vector  $C$  of the corresponding positive value.
- For example:  
+ 5  $\Rightarrow$  0101  
- 5  $\Rightarrow$  1101

#### 2. 1's Complement

- The leftmost bit is 0 for positive numbers and 1 for negative numbers
- Negative values are obtained by complementing each bit of the corresponding positive number.

#### For example:

For -3 we can find by complementing each bit in the vector 0011 to yield 1100.

- Same operation is used for converting a negative number to the corresponding positive value. The operation of forming the 1's complement of a given number is equivalent to subtracting that number from  $2^n-1$ .

#### 3. 2's Complement

- The leftmost bit is 0 for positive numbers and 1 for negative numbers.
- In this, forming the 2's complement of a number is done by subtracting that number from  $2^n$ .

Hence, the 2's complement of a number is obtained by adding 1 to the 1's complement of that number.

### 1.3.2 Arithmetic Addition

#### 1. In Signed-Magnitude form

- Follows the rules of ordinary arithmetic  
If the signs are same  $\Rightarrow$  add two magnitudes and give the sum common sign.

If the signs are different  $\Rightarrow$  subtract smaller magnitude from the larger and give the result, the sign of the larger magnitude.

**For Example:**

$$(+35) + (-37) = -(37-25) = -2$$

#### 2. In 2's complement form

- The system does not require a comparison or subtraction only addition and complementation is necessary.
- The procedure is as follows: Add the two numbers including their sign bits and discard any carry out of the sign (left most) bit position.

**Note:** The negative number must initially be in 2's complement and that if the sum obtained after the addition is negative, it is in 2's complement form.

**For Example:**

$$\begin{array}{r} 6 \quad 00000110 \\ +13 \quad 00001101 \\ \hline +19 \quad 00010011 \\ -6 \quad 11111010 \\ +13 \quad 00001101 \\ \hline +17 \quad 00000111 \end{array}$$

### 1.3.3 Arithmetic Subtraction

- Subtraction of two signed numbers, when negative numbers are in 2's complement form, subtraction is very simple and can be done as follows:
  - $\rightarrow$  Take the 2's complement of the subtrahend (including the sign bit)
  - $\rightarrow$  Add it to the minuend (including the sign bit)

$\rightarrow$  A carryout of the sign bit position is discarded.

- Changing a positive number to a negative number is easily done by taking its 2's complement and vice-versa is also true.

**For example:**  $(-6) - (-13) = +7$

In binary format, it is written as  $11111010 - 11110011$

The subtraction is changed to addition by taking the 2's complement of the subtrahend (-13) to give (+13).

In binary format this is

$$11111010 + 00001101 = 100000111$$

and removing the end carry, we obtain the answer as  $00000111 \Rightarrow (+7)$ .

### 1.3.4 Overflow in Integer Arithmetic

- In the 2's complement number representation system, n-bits can represent values in the range  $-2^{n-1}$  to  $+2^{n-1}-1$ .

When the result of an arithmetic operation is outside the representable range, an arithmetic overflow has occurred.

- While adding unsigned numbers, the carry out from the most significant bit position serves as the overflow indicator. This is not applicable for adding signed numbers.

**For example:**

By using 4-bit signed numbers, if we try to add the numbers +7 and +4, the output is  $1011 \Rightarrow -5 \Rightarrow$  Incorrect result (with carry-out = 0)

**Note:** Overflow may occur if both summands have the same sign. The addition of numbers with different signs cannot cause overflow.

- ❖ A single method to detect overflow is to examine the signs of two summands X and Y and the sign of the result. When both operands X and Y have the same sign, an overflow occurs when the sign of S is not the same as the signs of X & Y.



### 1.4 DECIMALFIXED-POINT REPRESENTATION

- The representation of decimal numbers in registers is a function of the binary code used to represent a decimal digit. A 4-bit decimal code requires four flip flops for each decimal digit.

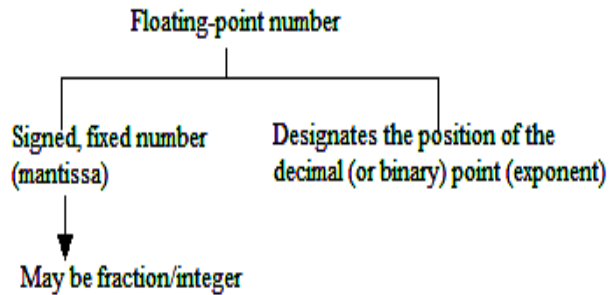
#### Disadvantages

- By representing numbers in decimal we are wasting amount of storage space since the number of bits needed to store a decimal number in a binary code is greater than the number of bits needed of its equivalent binary representation.
- The circuits required to perform decimal arithmetic are more complex.

#### Advantage

- In applications like business data processing we require small amounts of arithmetic computations (in decimal format).
- The representation of signed numbers in binary is similar to the representation of signed decimal numbers in BCD. The sign of a decimal number is usually represented with four bits to conform with the 4-bit code of the decimal digits.
- The signed-magnitude system is difficult to use with computers. The signed complement system can be either the 9's or the 10's complement is the one most commonly used. To obtain the 10's complement of a BCD number, we first take the 9's complement and then add one to the least significant digit. The 9's complement is calculated from the subtraction of each digit from 9.
- The subtraction of decimal numbers is either unsigned or in the signed-10's complement system. Take the 10's complement of the subtrahend and add it to the minuend.

### 1.5 FLOATING POINT REPRESENTATION



#### Example :

+ 6132.789

Fraction: +0.6132789

Exponents: +0.4

- Floating point is always interpreted to represent a number in the following form  $m \times r^e$   $m$  and  $e$  are physically represented in the register (including the signs). The radix  $r$  and the radix-point position of the mantissa are always assumed.

- A floating point binary number is represented in a similar manner except that it uses base-2 for exponent.

**For example:** The binary number + 1001.11 is represented with 8 bit fraction and 6 bit exponent as follows.

Fraction	Exponent
01001110	000100

- A floating point number is said to be normalized if the most significant digit of the mantissa is nonzero.

#### For example:

The decimal number 250 is normalized but 00035 is not.

Regardless of where the position of the radix point is assumed to be in the mantissa, the number is normalized only if its leftmost digit is nonzero.

The number can be normalized by shifting three positions to the left and discarding the leading 0's to obtain 11010000. Normalized numbers provide the maximum possible precision for the floating point number. A zero cannot be normalized in floating point by all 0's in the mantissa and exponent.

# GATE QUESTIONS

Topics	Page No
1. CACHE AND MAIN MEMORY	67
2. INSTRUCTIONS-PIPELINING & ADDRESSING MODES	76
3. CPU CONTROL DESIGN & INTERFACES	91
4. SECONDARY MEMORY & DMA	96



# 1

## CACHE AND MAIN MEMORY

**Q.1** A graphics card has on board memory of 1 Mbyte. Which of the following modes can the card not support?

- a) 1600 x 400 resolution with 256 colors on a 17 inch monitor
- b) 1600 x 400 resolution with 16 million colors on a 14 inch monitor
- c) 800 x 400 resolution with 16 million colors on a 17 inch monitor
- d) 800 x 800 resolution with 256 colors on a 14 inch monitor

[GATE-2000]

**Q.2** Which of the following requires a device driver?

- a) Register
- b) Cache
- c) Main memory
- d) Disk

[GATE-2002]

**Q.3** More than one words are put in one cache block to

- a) exploit the temporal locality of reference in a program
- b) exploit the spatial locality of reference in a program
- c) reduce the miss penalty
- d) None of the above

[GATE-2002]

**Q.4** Increasing the RAM of a computer typically improves performance because

- a) virtual memory increases
- b) larger RAM are faster
- c) fewer page faults occur
- d) fewer segmentation faults occur

[GATE-2005]

**Q.5** Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the Least

Recently Used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12, 0, 12, 8

- a) 2
- b) 3
- c) 4
- d) 5

[GATE-2006]

**Statements for Linked Questions no 6 & 7**

A CPU has a 32 Kbyte direct mapped cache with 128-Byte block size. Suppose

A is a two-dimensional array of size 512x 512 with elements that occupy 8-byte each. Consider the following two C code segments, P<sub>1</sub> and P<sub>2</sub>

P<sub>1</sub> :

```
for (i = 0; i < 512; i++) {
  for (j = 0; j < 512; j++) {
    x += A [i][j];
  }
}
```

P<sub>2</sub> :

```
for (i = 0; i < 512; i++) {
  for (j = 0; j < 512; j++) {
    x += A [j][i];
  }
}
```

P<sub>1</sub> and P<sub>2</sub> are executed independently with the same initial state, namely, the Array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by P<sub>1</sub> be M<sub>1</sub> and that for P<sub>2</sub> be M<sub>2</sub>.

**Q.6** The value M<sub>1</sub> is

- a) Zero
- b) 2048
- c) 16384
- d) 262144

[GATE-2006]

**Q.7** The value of the ratio  $\frac{M_1}{M_2}$  is

- a) Zero
- b)  $\frac{1}{16}$
- c)  $\frac{1}{8}$
- d) 16

[GATE-2006]

# EXPLANATIONS

**Q.1 (b)**

A graphics card with on board memory of 1 Mbyte cannot support a mode of 1600×400 resolution with 16 million colors on a 14 inch monitor.

**Q.2 (b)**

In computing, a device driver or software driver is a computer program allowing higher-level computer programs to interact with a hardware device.

A driver typically communicates with the device through the computer bus or communications subsystem to which the hardware connects. When a calling program invokes a routine in the driver, the driver issues commands to the device. Once the device sends data back to the driver, the driver may invoke routines in the original calling program. Drivers are hardware dependent and operating system specific. They usually provide the interrupt handling required for any necessary asynchronous time-dependent hardware interface.

**Q.3 (a)**

It is done to exploit the temporal locality of reference in a program as cache is the fastest memory available temporarily which is the mirror image of main memory and it stores more than a word at one time.

**Q.4 (c)**

We know that, size is directly proportional to page frame. So, the RAM is increased. The main memory also increases and thus the page frame size also increases which results in reduction of snapping.

Thus, lesser number of page faults occur. Now if any replacement rule is applied which doesn't cause blade anomaly always results in reduction of page faults.

**Q.5 (c)**

The page frames content after applying LRU for the sequence 8, 12, 0, 12, 8 is

	12	12	12	12
8	8	0	0	8
Miss	Miss	Miss	No Miss	Miss

Therefore, total number misses = 4

**Q.6 (c)**

16 array elements are brought into the cache as the first element A[0][0] is accessed and there will be hits for the next 15 accesses for A[0][0] to A[0][15] which are in cache and a miss at A[0][16], Therefore, there occurs 15 hits and one miss, for every  $512 \times 512 / 16 = 16384$  block transfer during P<sub>1</sub>.

**Q.7 (b)**

As the next element required to be accessed after A[0][0] is A[1][0], then the elements A[0][1] to A[0][15] brought into cache are of no use.

Thus, there will be 262144 (512 × 512) misses and no hits

Therefore,

$$M_1/M_2 = 16384/262144 = 1/16.$$

**Q.8 (a)**

Consider the following table, as it is given the following is concluded :

Tag	Set	Block
18	9	5

# ASSIGNMENT QUESTIONS

- Q.1** From a given tautology, another tautology can be delivered by interchanging  
 a) 0 and 1  
 b) AND and OR  
 c) 0 and 1; AND and OR  
 d) impossible to always derive
- Q.2** Which of the following logical operation produce a 0 if the inputs are 1, 1 and 0?  
 a) OR  
 b) AND  
 c) Exclusive-OR  
 d) Exclusive-NOR
- Q.3** Choose the correct answer.  
 If  $x$  is a Boolean variable, then  
 a)  $0 + x = x$                       b)  $1 \div x = x$   
 c)  $x + x = x$                         d)  $x + x' = 0$
- Q.4)** If  $X$ ,  $Y$  and  $Z$  are three Boolean variables then  
 a)  $X \cdot X' = 1$   
 b)  $X(Y + Z) = (X + Y)(X \div Z)$   
 c)  $X + XZ = X$   
 d)  $X + Y = Y + X$
- Q.5** Which of the following codes needs 7 bits to represent a character?  
 a) ASCII                                b) BCD  
 c) EBCDIC                              d) GRAY
- Q.6** Which of the following the are not weighted codes?  
 a) Roman number system  
 b) Decimal number system  
 c) Excess 3-code  
 d) Binary number system
- Q.7** The minimum time delay between the initiations of two independent memory operations is called  
 a) access time                      b) cycle time  
 c) transfer rate                      d) latency time
- Q.8** If  $X$ ,  $Y$  and  $Z$  are 3 Boolean variable then  $X(Y + Z)$  equals  $(X + Y)(X + Z)$ , if  $X$ ,  $Y$ ,  $Z$  take the values  
 a) 1, 0, 0                              b) 0, 1, 0  
 c) 1, 1, 0                              d) 0, 1, 1
- Q.9** Which of the following comments about the program Counter (PC) are true?  
 a) It is a register.  
 b) It is a cell in ROM.  
 c) During execution of the current instruction, its content changes.  
 d) None of the above
- Q.10** If  $(123)_5 = (A3)_{B'}$  then the number of possible value of  $A$  is  
 a) 4                                        b) 1  
 c) 3                                        d) 2
- Q.11** The speed imbalance between memory access and CPU operation can be reduced by  
 a) cache memory  
 b) memory interleaving  
 c) reducing the size of memory  
 d) none of the above
- Q.12** If  $(12A)_3 = (123)_{A'}$  then the value of  $A$  is  
 a) 3                                        b) 3 or 4  
 c) 2                                        d) none of the above
- Q.13** Choose the correct statement.  
 a) By scanning a bit pattern, one can say whether, it represents data or not.  
 b) Whether a given piece of information is a data or not depends on the particular application  
 c) Positive numbers can't be represented in 2's compliments form.  
 d) Positive numbers can't be represented in 1's compliments form.